OCP International Partnership — Open Core Protocol™

OVERVIEW

The Open Core Protocol (OCP) delivers the first *openly licensed, core-centric protocol* that comprehensively fulfills system-level integration requirements.

The OCP defines a comprehensive, bus-independent, high-performance and configurable interface between IP cores and on-chip communication subsystems.

A designer selects only those signals and features from the palette of OCP configurations needed to fulfill all of an IP core's unique data, control and test signaling requirements. Existing IP cores may be inexpensively adapted.

Defining a core interface using the OCP provides a complete description for system integration, and enables *core reuse and test reuse without rework.*

The OCP supports very high transfer performance, with data transfer models ranging from simple request-grant through pipelined request-response to more complex out-of-order operations.

OCP provides a clear delineation of design responsibility boundaries between core authors and SOC integrators.

HIGHLIGHTS

The OCP Promotes IP core reusability and reduces design time, design risk, and manufacturing costs for SOC designs.

The OCP is focused exclusively on the needs of an IP core; nothing about the OCP is bus or application specific.

- Enables IP core creation to be independent of system architecture and application design
- Describes *all* inter-core communications
- Optimizes die area by configuring into the OCP only those features needed by the core
- Timing guidelines assure IP core interoperability:
  - **Level 2** – highest performance interface timing
  - **Level 1** – conservative timing for effortless core connect
  - **Level 0** – protocol without timing specified (esp. useful for verification and simulation tools)

The full Open Core Protocol Specification is available at:
www.ocpip.org

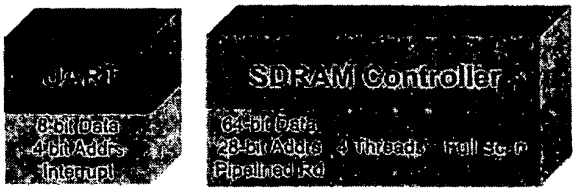
CAPABILITIES

The OCP captures all core characteristics without restricting system arbitration, address map, etc.

- Small set of mandatory signals, with a wide range of optional signals
- Core-specific data and address widths
- Structured method for inclusion of sideband signals: High-level flow control, interrupts, power control, device configuration registers, test modes, etc
- Synchronous uni-directional signaling allows simplified implementation, integration and timing analysis
- Transfers may be *pipelined* for reduced latency
- Optional burst transfers for higher efficiency
- Multiple concurrent transfer sequences may be managed with *thread identifiers*, for out-of-order completion
- A *connection identifier* may be used to provide end-to-end identification for targets desiring to distinguish initiators for service prioritization, etc
- OCP is a functional superset of the VSIA's Virtual Component Interface (VCI), adding configurable sideband control signaling and test harness signals

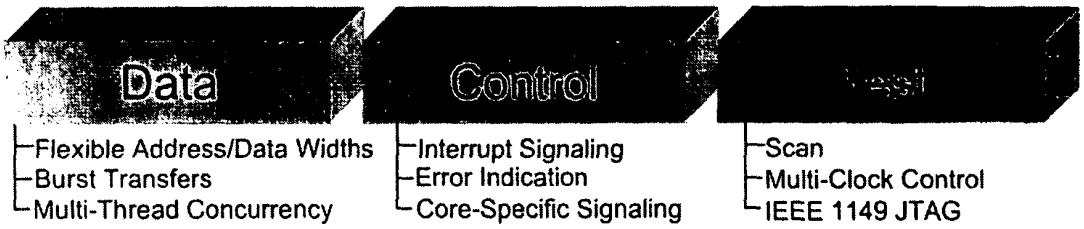
ADVANTAGES

- Eliminates the ongoing task of (re)defining interface protocols, then verifying, documenting, supporting them
- OCP readily adapts to support new core capabilities
- Test bench portability simplifies (re-)verification
- Limits test suite modifications for core enhancements
- Any bus structure can be interfaced to the OCP
- Delivers industry standard flexibility and reuse
- Symmetrical signaling enables direct point-to-point communication between 2 cores (without on-chip bus)



Very simple through highly complex core signaling can all be captured by this single protocol

Open Core Protocol™



KEY FEATURES

Basic OCP

- Master - slave interface with uni-directional signals
- Driven and sampled by the rising edge of the OCP clock
- Fully synchronous, no multi-cycle timing paths
- All signals are strictly point-to-point (except clock & reset)
- Simple request / acknowledge protocol
  - Supports data transfer on every clock cycle
  - Allows master or slave to control transfer rate
- Configurable data word width
- Configurable address width
- Pipelined or blocking reads
- Specific description formats for core characteristics, interfaces (signals, timing & configuration), performance

Simple Extensions – enhance Performance

- Burst codes link related transfers into complete transaction
- *Burst transactions* supported:
  - Sequential (defined or undefined length)
  - Streaming (FIFO)
  - Core-specific (cache lines)
- Pipelined (address ahead of data) writes
- Aligned or random byte enables
- Read data flow control
- Address space definition

Complex Extensions – enable Concurrency

- *Thread identifiers* enable:
  - Interleaved burst transactions
  - Out-of-order transaction completion
- Thread busy notification prevents interface blockin
- *Connection identifiers* enable:
  - End-to-end system initiator identification
  - Service priority management by system targets

Sideband Extensions – Dedicated Signaling

- Core-specific, user defined signals:
  - System event signals (e.g. interrupts, error noti
  - Synchronous reset
  - Data transfer coordination (e.g. high-level flow

Debug and Test Interface Extensions

- Support structured full or partial scan test environm
- *Scan* pertains to internal scan techniques for a pre-d hard-core or end user-inserted into a soft-core.
- *Clock Controls* are used for scan testing and debug, multiple clock domains
- *IEEE 1149* supports cores with a JTAG Test Acces
- Configurable for JTAG and Enhanced JTAG-based MIPS® (EJTAG), ARM®, TI® DSP, SPARC™ and o

CORECREATOR™

OCP-IP offers its members the use of an EDA tool created by Sonics, Inc. named CoreCreator™ to automate the tasks of building, simulating, verifying and packaging OCP-compatible cores. CoreCreator™ also supplies a protocol checker to ensure compliance with the OCP specification. IP core products can be fully componentized by consolidating core models, timing parameters, synthesis scripts, verification suites and test vectors.

OCP-IP:

OCP International Partnership Association, Inc. (OCP-IP) is an independent, non-profit semiconductor industry consortium formed to administer the support, promotion and enhancement of the Open Core Protocol (OCP). OCP-I is the first fully supported, openly licensed, comprehensive interface socket for semiconductor intellectual property (cores. The mission of OCP-IP is to address problems relating to design, verification and testing which are common t IP core reuse in system-on-chip (SOC) products. OCP-IP is funded through the annual membership dues of its members: intellectual property companies, integrated device manufacturers, system companies and design houses

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